# CS152: Section 2

### Q1. Iron Law

**Q1.1**: For each term in the Iron Law, give at least three techniques that improve that term.

Instructions/program:

Cycles/instruction:

Time/cycle:

**Q1.2**: Explain how each term changes given the proposed modification (increase / decrease / no effect).

[**Quiz 1, 2011**] In a classic RISC pipeline, modify the ISA (and thus the microarchitecture) to use hardware interlocking instead of software interlocking for both branch delay slots and load-use delay slots

Instructions/program:

Cycles/instruction:

Time/cycle:

[**Quiz 1, 2013**] Remove hardware floating-point instructions and instead use software subroutines for floating-point arithmetic

Instructions/program:

Cycles/instruction:

Time/cycle:

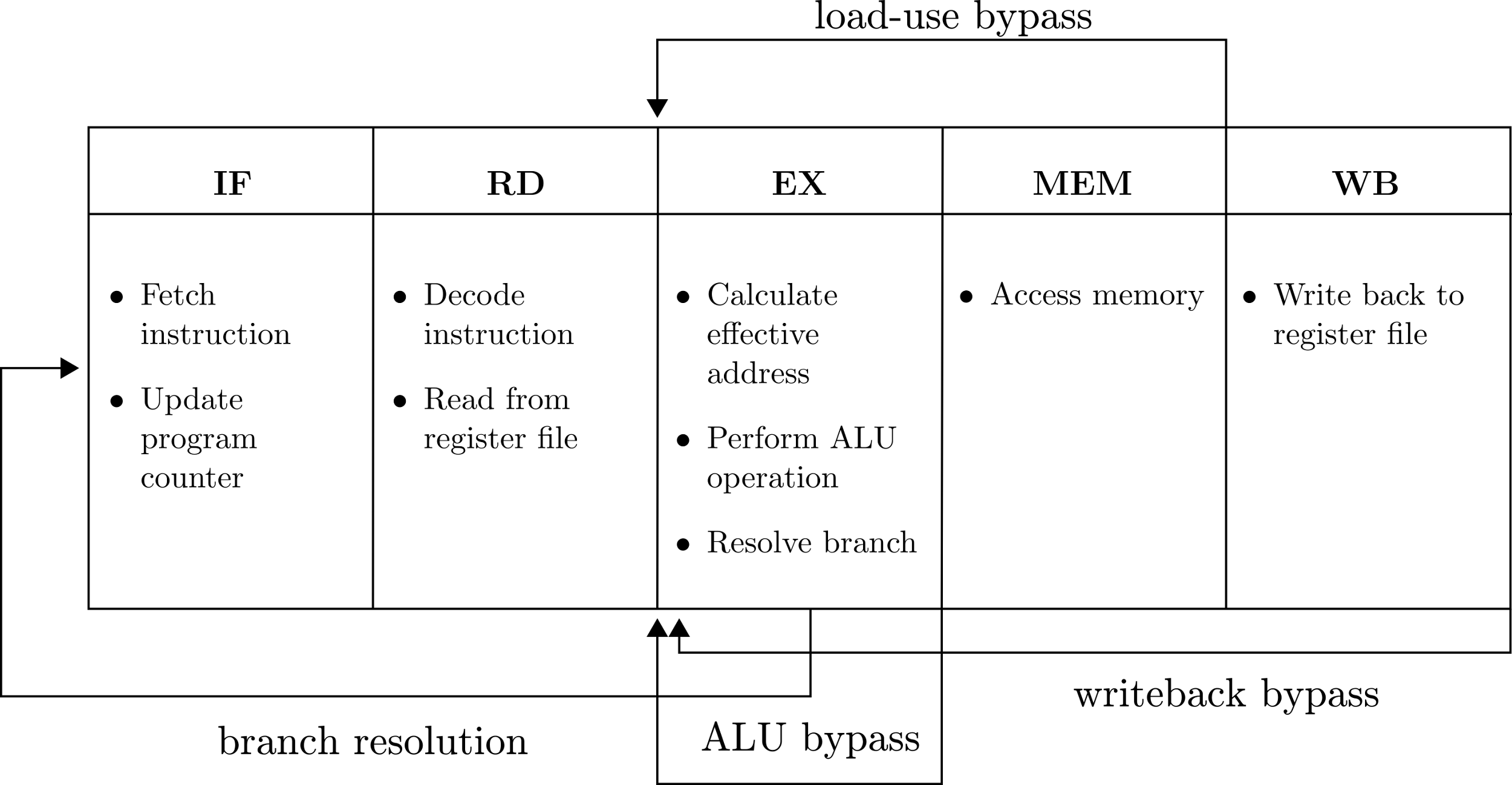
### Q2. Pipelining

**Q2.1**: What does the following code do? How many iterations does it run?

ADDI x2, x0, 0x700  
LOOP: ADD x1, x2, x0  
 LW x2, 4(x2)  
 BNE x2, x0, LOOP

| **Memory Address** | **Memory Value** |
| --- | --- |
| 0x400 | 0x000 |
| 0x404 | 0xD40 |
| ... |  |
| 0x700 | 0x9F0 |
| 0x704 | 0x400 |
| ... |  |
| 0x9F0 | 0x400 |
| 0x9F4 | 0x000 |
| ... |  |
| 0xD40 | 0x000 |
| 0xD44 | 0x9F0 |

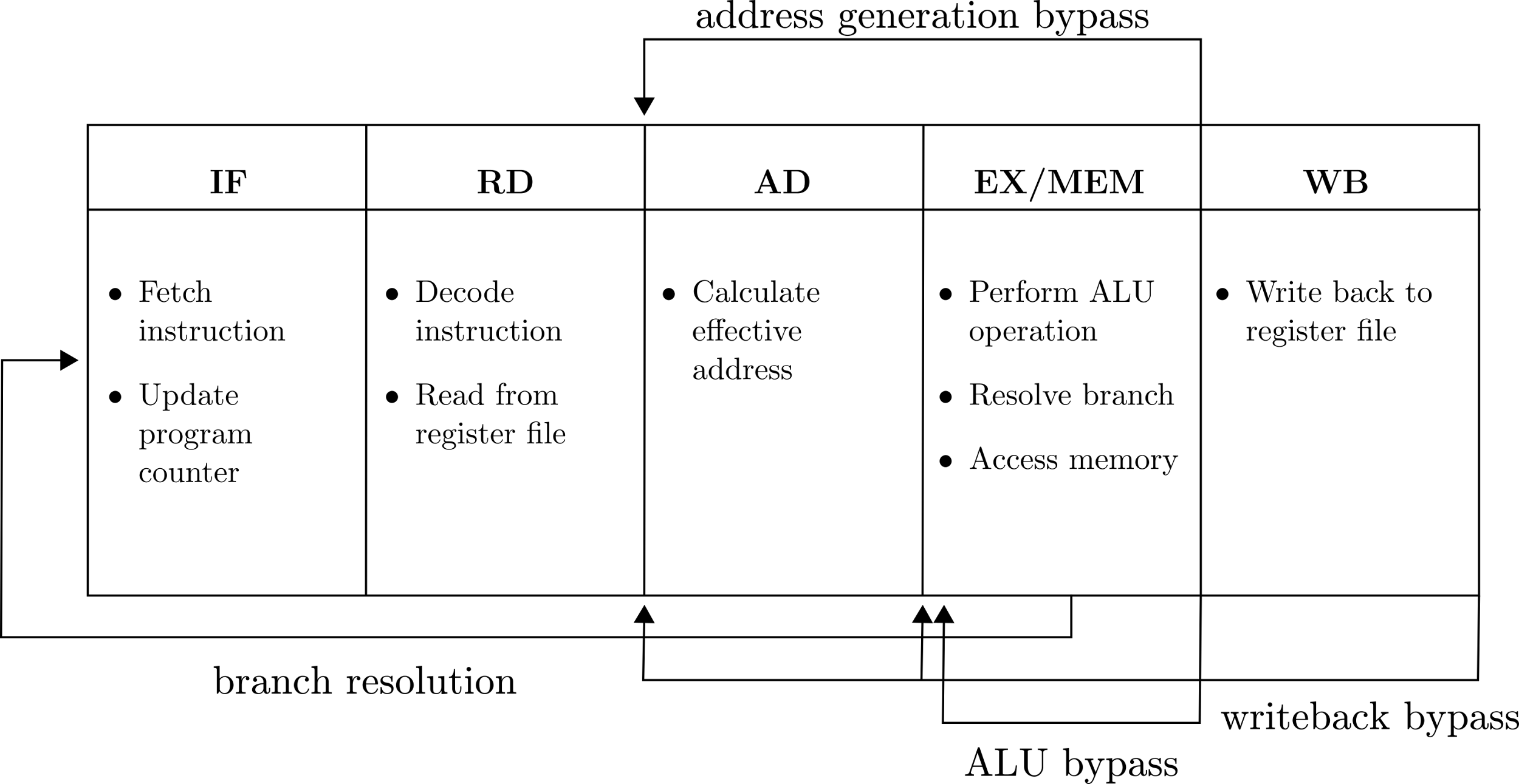
**Q2.2**: Fill out the pipeline diagram for the following pipeline, assuming that branches are always predicted not taken.



* What is the CPI for the given code sequence?

* Consider splitting MEM into two stages, M1 and M2. How does the CPI change?
* What is the CPI if the BNE is always correctly predicted?

**Q2.3**: Fill out the pipeline diagram for the following pipeline, assuming that branches are always predicted not taken. [M. Golden and T. Mudge, "A comparison of two pipeline organizations", 1994]



* What is the CPI for the given code sequence?
* Consider splitting EX/MEM into two stages, M1 and EX/M2. How does the CPI change?
* What is the CPI if the BNE is always correctly predicted?

**Q2.4**: Suppose that the “load-use interlock” (LUI) pipeline from Q2.2 meets timing at 1 GHz. What is the minimum frequency at which the “address-generation interlock” (AGI) pipeline from Q2.3 performs better on the given code sequence, assuming perfect branch prediction?

**Q2.5:** Under what circumstances might you consider using the AGI pipeline design over the LUI pipeline?

**Q2.2: Load-Use Interlock (LUI) pipeline**

|  | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** | **16** | **17** | **18** | **19** | **20** | **21** | **22** | **23** | **24** | **25** | **26** | **27** | **28** | **29** | **30** |
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| addi | F | D | X | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| add |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| lw |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| bne |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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**Q2.3: Address Generation Interlock (AGI) pipeline**

|  | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** | **16** | **17** | **18** | **19** | **20** | **21** | **22** | **23** | **24** | **25** | **26** | **27** | **28** | **29** | **30** |
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| addi | F | D | A | X | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| add |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| lw |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| bne |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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